**BSIM MODEL FOR NANO-WIRE FET**

AISHWARYA NAG

ABHIMANYU MAGAPUhorizontal line

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# Introduction

This project is on compact modelling of a Nano-wire FET(NWFET) based on TCAD model data.

The primary objective was to assess whether the CFET model offers improvements over the UMC\_180 nm technology node, specifically regarding speed, delay, and power dissipation in essential digital circuit elements.

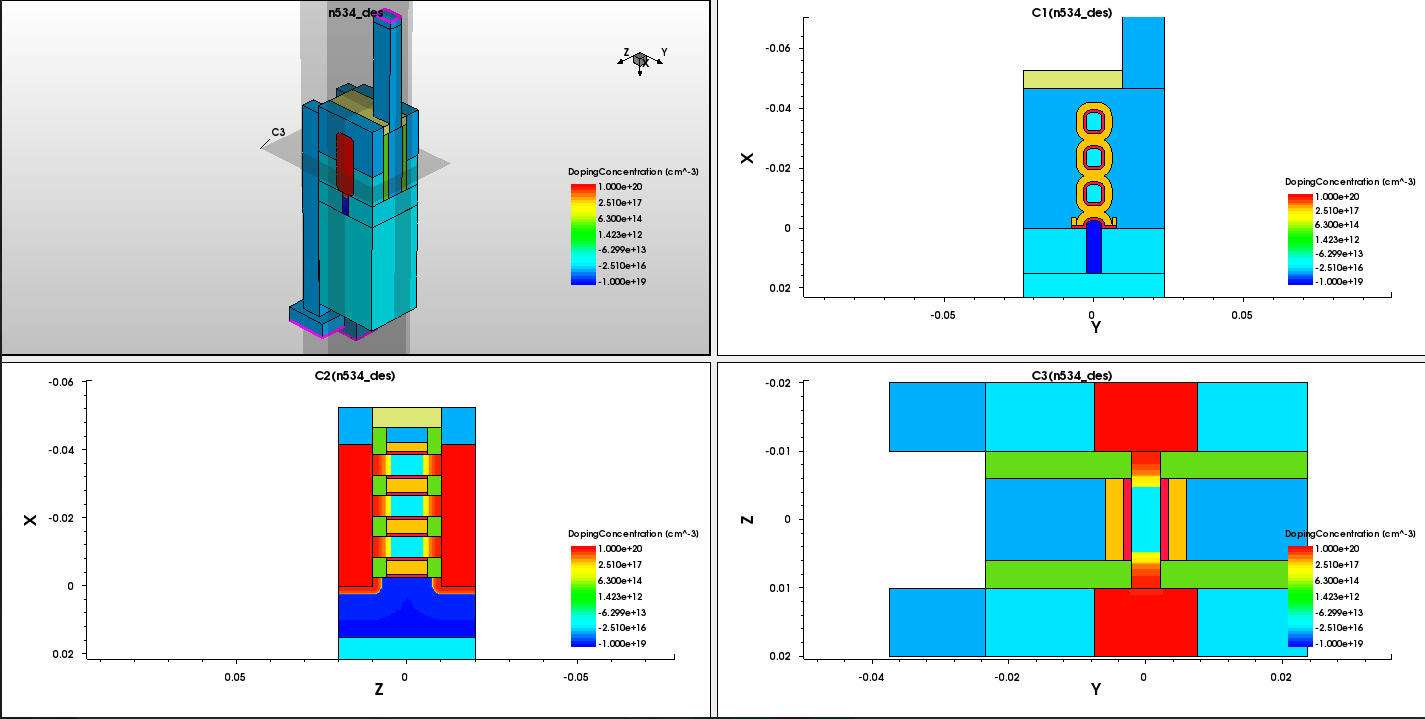
The model was carefully calibrated, with critical parameters adjusted to ensure accurate representation; all other parameters not mentioned were retained at their default values. The fitting procedure and steps followed in this project have been written down in detail, and all assumptions have been stated.

For this project, we used the latest version of BSIM-CMG available at the project’s start (V111.2.0) to model the NWFET. The I-V and C-V characteristics were individually fitted, with goodness-of-fit metrics calculated to ensure accuracy. Python, Desmos and MATLAB were utilized extensively for curve fitting and parameter extraction.

The BSIM starter file with the manual and the skeleton code is available on the official Berkeley Website: <https://www.bsim.berkeley.edu/models/bsimcmg/>

Besides the BSIM-CMG manual, we also used “*FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard* ” as a reference.

# Device Characteristics

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*Device Type* Bulk Silicon GAAFET

*GAA Body* 3 GAA bodies placed one on top of the other along y axis (Fig 1.3)

*Fins* 1 fin comprises of 3 GAA bodies stacked one on top of the other

*Fingers* Each FET is referred to as one finger

*Dielectric Material* HfO2

*Gate* TiN Material with 2 sided contact

*Substrate* Si Material with no overlap between substrate and source/drain

**PMOS NMOS**

*Channel Material* 70% Silicon 30% Germanium Silicon

The device was designed for a VDD of 0.7V and a gate length ranging from 10nm to 16nm.

The number of channels and fins were aso varied and taken into account while modelling the FET.

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# Extracted Parameter List

| Parameter | NMOS | PMOS | Unit | Description |
| --- | --- | --- | --- | --- |
| L | 10 to 22 | 10 to 22 | nm | Designed Gate Length |
| TFIN | 1.5e-8 | 1.5e-8 | m | Fin Thickness |
| FPITCH | 2e-8 | 2e-8 | m | Fin pitch (distance between two fins) |
| NFIN | 1 to 4 | 1 to 4 | - | Number of fins per finger |
| NGCON | 2 | 2 | - | Number of gate contact (1 or 2 sided) |
| ASEO | 0 | 0 | m2 | Source-to-substrate overlap area through oxide |
| ADEO | 0 | 0 | m2 | Drain-to-substrate overlap area through oxide |
| PSEO | 0 | 0 | m2 | Perimeter of source-to-substrate overlap region through oxide |
| PDEO | 0 | 0 | m2 | Perimeter of drain-to-substrate overlap region through oxide |
| ASEJ | 232e-18 | 232e-18 | m2 | Source junction area |
| ADEJ | 232e-18 | 232e-18 | m2 | Drain junction area |
| PSEJ | 74e-9 | 74e-9 | m | Source-to-substrate PN junction perimeter |
| PDEJ | 74e-9 | 74e-9 | m | Drain-to-substrate PN junction perimeter |
| LRSD | 12e-9 | 12e-9 | m | Length of the source/drain |
| TGAA | 4e-9 | 4e-9 | m | Thickness of individual GAA bodies |
| TSUS | 4e-9 | 4e-9 | m | Separation between GAA bodies" |
| HPFF | 2.5e-9 | 2.5e-9 | m | Fin-height of parasitic finFET |
| WGAA | 8e-9 | 8e-9 | m | GAA body width |
| DWS | 0 | 0 | m | Total width correction for GAA body |
| DACH | 0 | 0 | m2 | Total area correction for GAA body |
| NGAA | 1 to 5 | 1 to 5 | - | Number of GAA bodies per fin |
| NF | 1 | 1 | - | Number of fingers |
| TYPE | 1 | -1 | - | 1: NMOS; -1: PMOS |
| BULKMOD | 1 | 1 | - | Bulk type |
| GEOMOD | 5 | 5 | - | Model type |
| CGEO1SW | 0 | 0 | - | Capacitance unit selector |
| RDSMOD | 0 | 0 | - | Resistance Model |
| CVMOD | 1 | 1 | - | I-V, C-V coupling |
| CGEOMOD | 0 | 0 | - | Capacitance geometry |
| RGEOMOD | 0 | 0 | - | Resistance geometry |
| EOT | 1.625e-10 | 1.625e-10 | m | Equivalent oxide thickness |
| TOXP | 1e-9 | 1e-9 | m | Physical oxide thickness |
| HFIN | 26.5e-9 | 26.5e-9 | m | Fin height |
| NSD | 1e26 | 1e26 | /m3 | Source/drain active doping concentration |
| LINT | 0 | 0 | m | Length reduction parameter (dopant diffusion effect) |
| EPSROX | 24 | 24 | - | Relative dielectric constant of the gate dielectric |
| EPSRSUB | 11.8 | 13.06 | - | Relative dielectric constant of the channel material |
| NI0SUB | 1.1e16 | 5.11e18 | /m3 | Intrinsic carrier constant at 300.15K |
| BG0SUB | 1.12 | 1.12 | eV | Bandgap of substrate at 300.15K |
| NC0SUB | 2.86e25 | 2.5e25 | /m3 | Conduction band density of states |
| EASUB | 4.05 | 4.05 | eV | Electron affinity of substrate |
| NBODY | 1e22 | 1e22 | /m3 | Channel (body) doping |
| PHIG | 4.38 | 4.86 | eV | Gate workfunction |
| NGATE | 0 | 0 | /m3 | Poly gate doping |
| DVTP0 | 0 | 0.117063 | - | Coefficient for drain-induced Vth shift (DITS) |
| DVTP1 | 0 | 0.007926 | - | DITS exponent coefficient |
| CDSC | 7e-3 | 7e-3 | F/m2 | Coupling capacitance between S/D and channel |
| CDSCD | 4e-1 | 0.01 | F/m2 | Drain-bias sensitivity of CDSC |
| DVT0 | 4.783406 | 4.222682 | - | SCE coefficient |
| DVT1 | 3.419185 | 0.201257 | - | SCE Exponent coefficient |
| DVT1SS | 3.419185 | 0.201257 | - | Subthreshold swing exponent coefficient |
| ETA0 | 0.092639 | 0.003119 | - | DIBL coefficient |
| DSUB | 0.097 | 0.019829 | - | DIBL exponent coefficient |
| K1RSCE | -0.285562 | -1.195107 | V0.5 | K1 for reverse short channel effect calculation |
| QMTCENCV | 13 | 25 | - | Prefactor + switch for QM Width and Toxeff correction for CV |
| VSAT | 8.54e7 | 8.54e7 | m/s | Saturation velocity for the saturation region |
| KSATIV | 1.185 | 1.25 | - | Parameter for long channel Vdsat |
| U0 | 3e-2 | 3e-2 | m2/Vs | Low field Mobility |
| ETAMOB | 14 | 0.01 | - | Effective field parameter |
| UP | 0.3 | 0 | umLPA | Mobility L coefficient |
| UA | 0.3 | 0.1 | (cm/MV)EU | Phonon/surface roughness scattering parameter |
| EU | 0.93 | 0.3 | cm/MV | Phonon/surface roughness scattering parameter |
| RDSWMIN | 47 | 100 | ohm\*umWR | RDSMOD = 0 S/D extension resistance per unit width at high Vgs |
| ARDSW | 326.748 | 556.16 | - | Pre-exponential coefficient for RDSW |
| BRDSW | 8.0871e-9 | 5.93e-9 | - | Exponential coefficient for RDSW |
| RDSW | 16.7289 | 192.724 | ohm\*umWR | RDSMOD = 0 zero bias S/D extension resistance per unit width |
| WR | 1 | 1 | - | W dependence parameter of S/D extension resistance |
| LSP | 5e-9 | 5e-9 | m | Thickness of the gate sidewall spacer |
| CFS | 2.5e-10 | 2.403e-10 | F/m | Outer fringe capacitance at source side |
| CFD | 2.472e-10 | 2.389e-10 | F/m | Outer fringe capacitance at drain side |
| ETA0CV | 0.65 |  | - | C-V DIBL coefficient |
| U0CV | U0 | U0 |  | C-V Low field Mobility |
| UACV | UA | UA |  | C-V Phonon/surface roughness scattering parameter |
| UCCV | UC | UC |  | C-V Body effect |
| UDCV | UD | UD |  | C-V coulomb scattering |
| VSATCV | VSAT | VSAT |  | C-V velocity saturation |
| PQM | 0.287 |  |  | Slope of Tcen in inversion |
| QM0 | 1e-6 |  | V | Knee-point for Tcen in inversion |

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# Extraction Procedure

## Physical Parameters

L Length is varied from 10nm to 22nm to find length dependence

TFIN Thickness of circular fin measured along y axis

FPITCH Distance between 2 fins in case of multiple fins

NFIN Varied based on number of parallel fins with stacked GAA bodies

ASEO, ADEO 0 since no overlap in the case of gate all around FET bodies

PSEO, PDEO

ASEJ, ADEJ 29nm x 8nm = 232nm2

PSEJ, PDEJ 2 x (29nm + 8nm) = 74nm

TGAA, TSUS, Extracted from Sentaurus Model of device per GAA body

HPFF, WGAA

DWS, DACH Assumed to be 0 based on the Sentaurus Model

NGAA Number of GAA bodies per fin stacked vertically is varied

GEOMOD Set as 5 for gate all around FET

BULKMOD Set as 1 for Bulk Silicon

TOXP Extracted from Sentaurus

EOT Physical Oxide Thickness x SiO2 HfO2 = 1nm x 3.9 24

HFIN Height of fin measured along x axis

NSD, NBODY Extracted from Sentaurus

EPSROX Dielectric constant of HfO2

EASUB Electron Affinity of Si

EPSRSUB For NMOS: dielectric constant of Si

For PMOS: dielectric constant of Six0.7 + dielectric constant of Gex0.3

NI0SUB For NMOS: intrinsic carrier concentration of Si

For PMOS: intrinsic carrier concentration of Si x 0.7 +

intrinsic carrier concentration of Ge x 0.3

NC0SUB For NMOS: conduction band DOS of Si

For PMOS: conduction band DOS of Si x 0.7 +

conduction band DOS of Ge x 0.3

BG0SUB Bandgap of Silicon substrate

NGATE Metal Gate used hence set to 0

COVS, COVD Since no overlap area between substrate and source/drain

For cadence simulations, minute changes in effective width due to change in shape of fin can be controlled externally using parameter DELTAW where effective width = width calculated from dimension and number of fins + DELTAW

A similar change can be introduced just for CV plots without disturbing IV plots using the parameter DELTAWCV

Carrier mobility can be controlled using parameter U0MULT

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## Vth Parameters

To model the shift in threshold voltage (Vth) due to changes in transistor length and drain-source voltage (VDS), parameters DVT0, DVT1, ETA0, DSUB, DVTP0, DVTP1, PHIG and K1RSCE were used.

PHIG is inversely dependent to Vth. The value of PHIG was extracted independently for PMOS and NMOS to match the TCAD I-V simulations for device length of 16nm using trial and error.

The Vth values from TCAD simulations for various transistor lengths at two specific VDS values: 0.5V and 0.7V were then extracted. For each VDS value, the highest Vth value—corresponding to the longest transistor length—was taken as the reference threshold voltage, Vth0. The differences, or “delta” values, between Vth0 and Vth for shorter lengths were calculated. Since the threshold voltages for the shorter lengths were smaller than Vth0, these delta values were negative.

With these delta values for the two VDS values, data points were plotted and fitted to polynomial functions on Desmos. A high-degree polynomial was chosen to ensure an accurate fit. These fitted polynomial equations were then used in a MATLAB script that simultaneously fits the Vth data for both VDS values (0.5V and 0.7V) for all lengths. In the MATLAB code, we used a large number of sweep points ( ~2,000, 000) to ensure an accurate fit.

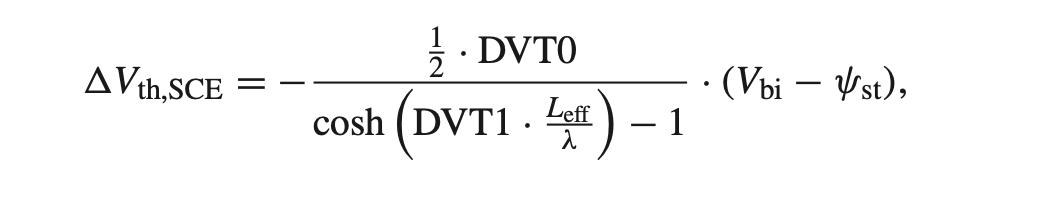
Parameters DVT1 and DVT0 contribute to changes in Vth due to short channel effect. Hence, they are extracted from the length dependence of Vth.

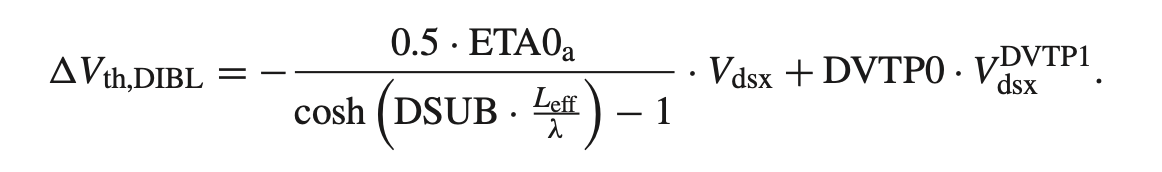
Parameters ETA0, DVTP0, DSUB and DVTP1 cause changes in Vth due to drain induced barrier lowering. Hence, they are extracted from the drain voltage dependence of Vth.

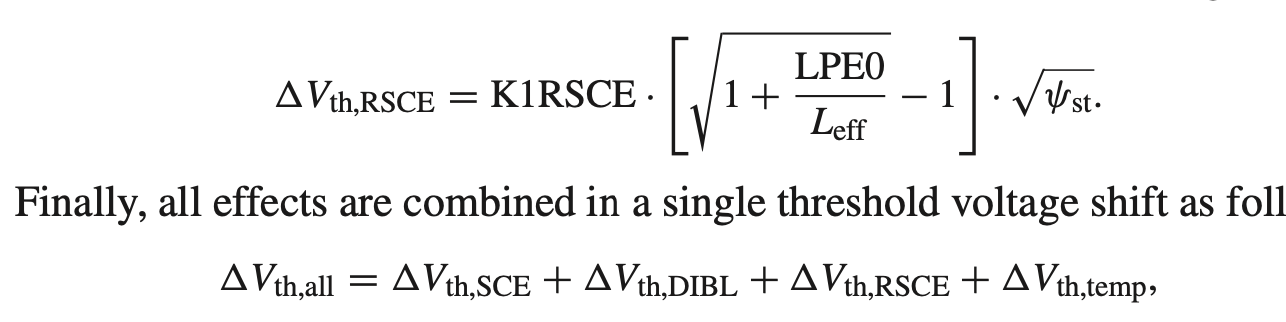
K1RSCE is used in reference to reverse short channel effect. It overcomes the effect of SCE caused by DIBL which decreases Vth. It is done by adding extra doping near the source and drain region. For BSIM, K1RSCE replicates this phenomenon in the mathematical equations without extra physical source drain doping to get accurate values of threshold voltage.

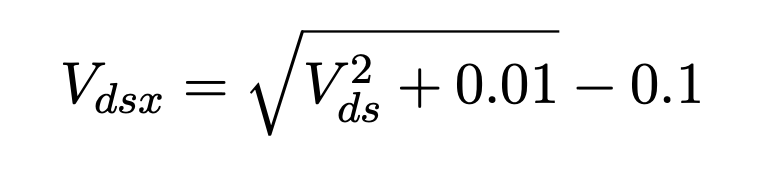
Inverse proportionality of conduction band density of states of the channel and threshold voltage has also been observed.

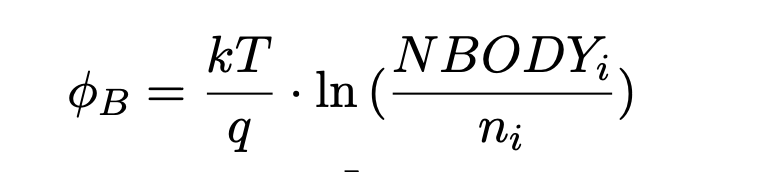
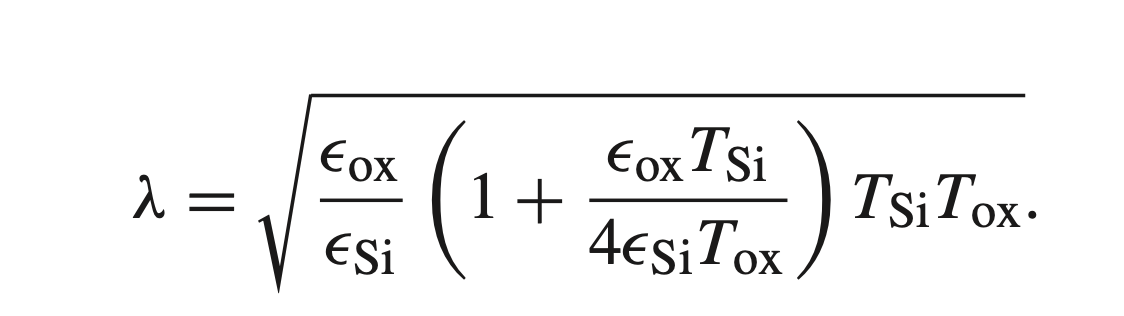
The following equations were used to fit the data -

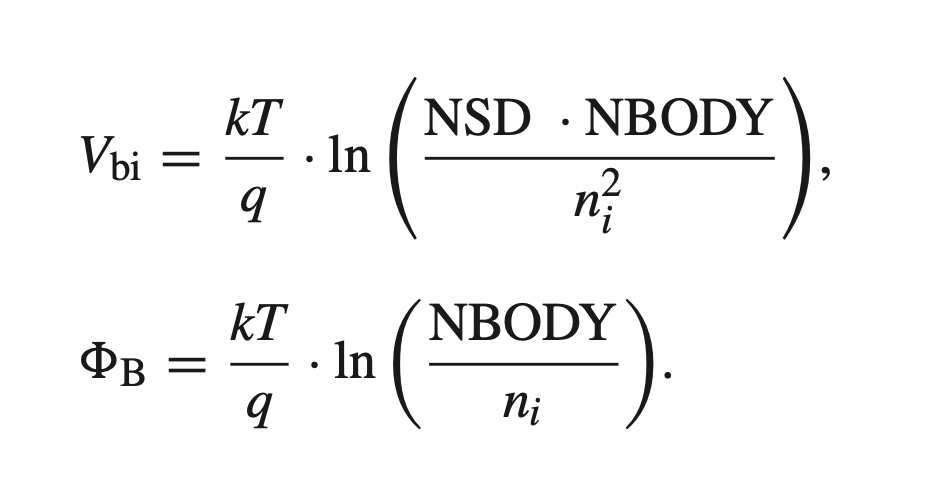










Parameters not mentioned are set to their default values.

In cadence simulations, variations in vth can be introduced using the parameter DELVTRAND. It increments vth to default value + DELVTRAND and can be used to analyse process variations.

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## Scaling Parameters

Next, I-V plots were fit to match the TCAD simulation I-V plots with respect to on-state and off-state magnitudes using UA, EU, KSATIV, CDSCD, RDSW and VSAT. The length dependence of I-V was introduced using ARDSW and BRDSW.

An inverse relationship was observed between parameters UA and EU, and the current magnitude of the graphs. UA and EU are responsible for phonon scattering in case of a rough surface. Reducing the scattering caused an increase in the magnitude of current. An increase from order e-9 to e-6 was observed. This was used to fit the magnitude for Vds = 0.05V.

This was followed by fitting the magnitude of current for the saturation region with Vds = 0.7V. Parameters KSATIV, CDSCD and VSAT showed variation in magnitude of current for saturation region leaving the graph of linear region completely unchanged. KSATIV is responsible for velocity saturation in long channel FETs. It has inverse dependence on magnitude. CDSCD increases the drain sensitivity of source/drain and channel coupling. Hence, CDSCD was increased from the default value to increase the magnitude of current. VSAT is the velocity saturation parameter which is directly proportional to the magnitude of current.

This provided a good fit I-V graph for both linear and saturation region for 10nm gate length.

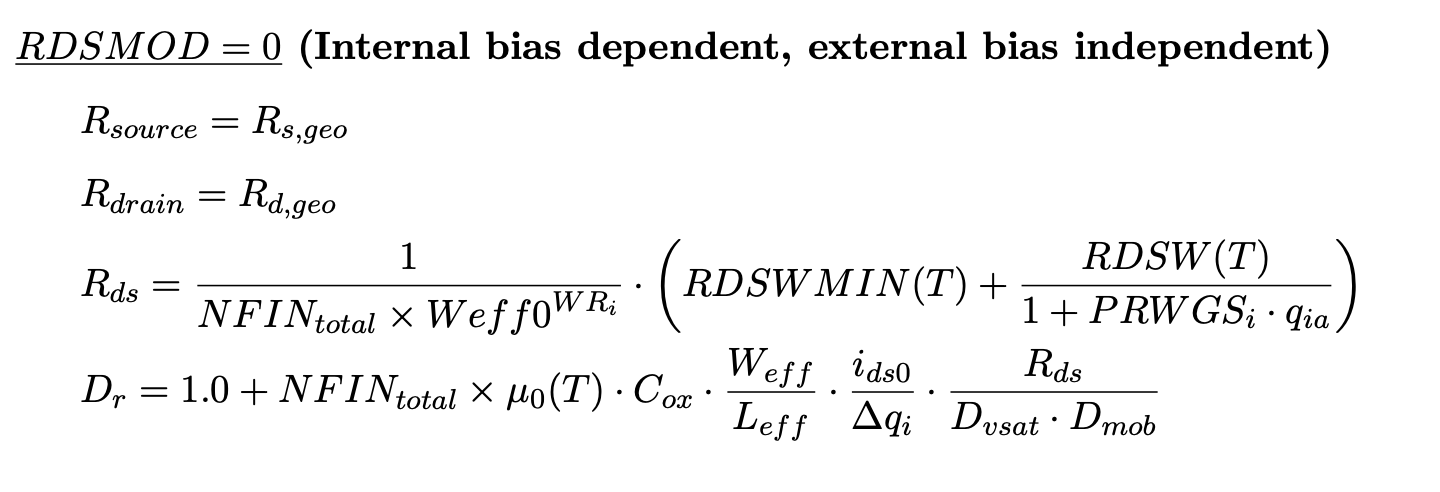
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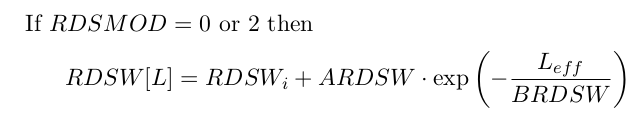
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## Parasitic Resistance Parameters

The total parasitic resistance at the source/drain terminal consists of two parts: Bias independent and Bias dependent. RDSMOD was set to 0, which made bias dependent part of parasitic resistance internal to the model, while bias independent part external to the model.



To introduce length dependence, the following formula was used:



For RDSMOD = 0, the model’s drain-source resistance (Rds) is governed by two parameters: RDSWMIN and RDSW. Initially, RDSWMIN was assigned a constant value, with the option to adjust it later if needed.

Next, RDSW[L] value was extracted for different lengths to match cadence simulations with TCAD simulations. RDSW represents resistance. Hence, an increase in its value reduces the magnitude in the saturation region. The data of different RDSW[L] corresponding to different lengths was fed into DESMOS with the equation above to fit the data and output the best possible RDSW, ARDSW and BRDSW

In all equations, Leff has been assumed to be equal to gate length with no length reduction due to dopant diffusion effect or offset due to mask/etch effect.

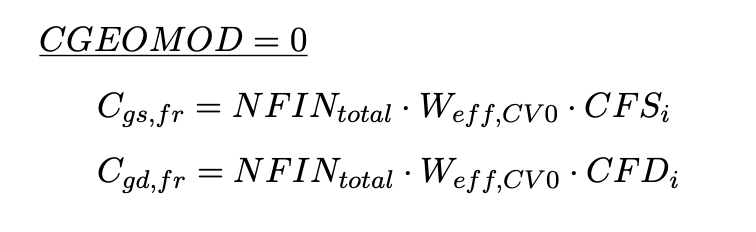
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## Parasitic Capacitance Parameters

To fit the capacitance, the I-V and C-V curves were coupled by setting CVMOD = 1. This configuration aligns capacitance parameters (like ETA0CV, UACV) with their I-V counterparts (ETA0, UA) by default.

The unit selector CGEO1SW was set to 0, making all capacitance units in Farads.

For fringing capacitance, only the bias-independent outer fringing capacitance was modeled. When CGEOMOD = 0, the fringe and overlap capacitances are proportional to the number of fins and effective width. Setting CGEOMOD = 1 introduces additional parasitic capacitance parameters, such as CFS, CFD, CDSP, COVS, and COVD.



To determine CFS, the CGS value from TCAD at VGS = 0V and VDS = 0.7V was divided by the effective width (72 nm). CFD was similarly calculated using CGD data. The constant drain-to-source capacitance was obtained from the simulated CSD curve at VGS = 0V and Vds = 0.7V.

Quantum effects were enabled for the C-V curve using QMTCENCV. A trial-and-error approach was then applied to adjust the model, fitting CGG (sum of CGS and CGD) to match the TCAD data.